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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/177,572	10/23/98	TERASHIMA Y	35.C13035

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WM02/0226

EXAMINER	
NGUYEN, K	
ART UNIT	**PAPER NUMBER**
2674	9

DATE MAILED: 02/26/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/177,572	TERASHIMA ET AL.	
	Examiner	Art Unit	
	Kevin M. Nguyen	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/7/2000* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)
16) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
18) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other: .

DETAILED ACTION

1. The amendment filed on 12/7/2000 is entered. The rejection of claims 1-12 are maintained.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Iwasaki (4,745,485).

4. As to claims 1, 6, 7 and 11, Iwasaki teaches a memory controller which includes data signal input from the S/P converter 2 converts the serial video signal to a parallel signal for every eight bits. The parallel video signal converted by the S/P converter 2 is supplied to a latch circuit 3. The latch circuit 3 is supplied to frame memories 4 and 5, a latch circuit 6 for the data read out (see figure 1, column 3, lines 18-29). The picture element data is displayed with good quality on the liquid crystal display (10) by using the frame memories (4 and 5) corresponding to one frame (see abstract). Accordingly, the latch circuit 3 corresponds to the FIFO as claimed.

5. As to claim 2, Iwasaki teaches frame memories 4 and 5 are controlled by the two-phase clock signal $\phi 1$ (fig. 2(d)) and $\phi 2$ (fig.2(e)) provided from the timing control circuit 13 so that the write state and the read state of the stored content are selected

alternately by the clock signal $\phi 1$. The write address counter 15 and the read address counter 16 and 17 are respectively make to count in synchronism with the clock signal $\phi 2$.

6. As to claims 3-5 and 8-10, Iwasaki teaches the serial clock frequency of the S/P converter 2 is equal to twice the serial clock frequency of the P/S converters 7 and 8. Since the video signal is serial data, the latter half of the n-1th frame and the first half of the nth are continuous (column 9, lines 54-64). The bit width of input data for every 8 bits by the S/P converter 2 (column 4, lines 44-45) and the video signal of the first frame corresponding to the upper display area 11 the address thereof being 1FFFF (see figure 1, column 5, lines 48-54 and column 6, lines 28-35).

7. As to claim 12, Iwasaki teaches the driver 9 drives the liquid crystal display 10 (see figure 1, column 3, lines 51-52), a memory controller which includes data signal input from the S/P converter 2 converts the serial video signal to a parallel signal for every eight bits. The parallel video signal converted by the S/P converter 2 is supplied to a latch circuit 3. The latch circuit 3 is supplied to frame memories 4 and 5, a latch circuit 6 for the data read out (see figure 1, column 3, lines 18-29). The picture element data is displayed with good quality on the liquid crystal display (10) by using the frame memories (4 and 5) corresponding to one frame (see abstract). Accordingly, the latch circuit 3 corresponds to the FIFO as claimed.

Response to Arguments

8. Applicants argues that in claim 1 recites "a memory controller including a serial/parallel converter section for converting serial input data into parallel data, an

FIFO memory section for temporarily storing converted data, a memory section connected to the FIFO memory section to store data for a frame and a second FIFO memory section for temporarily storing the data read out from the frame memory section. Claim 6 recites controller including a serial/parallel converter section for performing a serial/ parallel conversion of converting a-bit data, an FIFO memory section for temporarily storing converted axn-bit data, a memory section connected to the FIFO memory section to store data for a frame and a second FIFO memory section for temporarily storing the axn-bit data read out from the frame memory section. Claim 12 recites "wherein said decoder includes a memory controller comprising a serial/parallel converter section for converting serial input data into parallel data, an FIFO memory section for temporarily storing converted data, a memory section connected to the FIFO memory section to store data for a frame and a FIFO second section for temporarily storing the data read out from the frame memory section." These argument are not persuasive because Iwasaki's invention teaches the picture element data is displayed with good quality on the liquid crystal display (10) by using the frame memories (4 and 5) corresponding to one frame (see abstract). These arguments are not persuasive because Kuwata et al. (5,900,857) teaches the structure of memory controller in employed in order to reduce memory capacity as possible were very well known in the art (see fig.15, col. 4, lines 39-47 of Kuwata et al.).

For these reasons, the rejections of claims 1-12 based on Iwasaki have been maintained.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See PTO-892 form.

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin M. Nguyen whose telephone number is 703-305-6209. The examiner can normally be reached on MON-FRI from 9:00-5:00 with alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard A Hjerpe can be reached on 703-305-4709. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-6606 for regular communications and 703-308-6606 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-4700.

Kevin M. Nguyen
Examiner
Art Unit 2674

KN
February 23, 2001

RICHARD HJERPE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600